S'12:7AN:EC 407 (1482)

DESIGN OF ELECTRONIC DEVICES AND CIRCUITS

Time : Three hours

Maximum Marks : 100

Answer FIVE *questions, taking* ANY TWO *from* **Group A,** ANY TWO *from* **Group B** *and* ALL *from* **Group C.**

All parts of a question (a,b,etc.) should be answered at one place.

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Group A

1. (*a*) For the amplifier circuit, shown in Fig. 1, $R_1 = 10\ k\Omega$, $R_f = 100\ k\Omega$, $V_i = 1$ V. A load of 25 kΩ is connected to the output terminal. Calculate (*i*) i_1, (*ii*) V_0, (*iii*) I_L and total current i_0 into the output pin. **8**

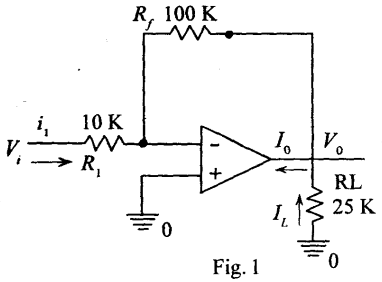

Fig. 1

(*Turn Over*)

(*b*) What are the characteristics of ideal operational amplifier? 3

(*c*) Explain how constant current source circuit improves the CMRR of the op amp. 9

2. (*a*) Explain the operation of full-wave rectifier with a neat diagram and obtain the expression for rectifier efficiency η. 10

(*b*) A half-wave rectifier is used to supply 24 V d.c. to a resistive load of 500 Ω and the diode has a forward resistance of 50 Ω. Calculate the maximum value of the a.c. voltage required at the input. 6

(*c*) What is meant by peak inverse voltage in rectifiers? 2

(*d*) What is regulated power supply? 2

3. (*a*) Explain about the operation of series op amp regulator with a neat block diagram. 8

(*b*) Describe the characteristics of IC voltage regulators. 4

(*c*) In Fig. 2, let $V_{EB(ON)} = 1$ V, $\beta = 15$, $V_L = 5$V. Calculate the output current coming from 7805 and I_C coming from transistor Q_1 for loads 100 Ω and 5 Ω. 8

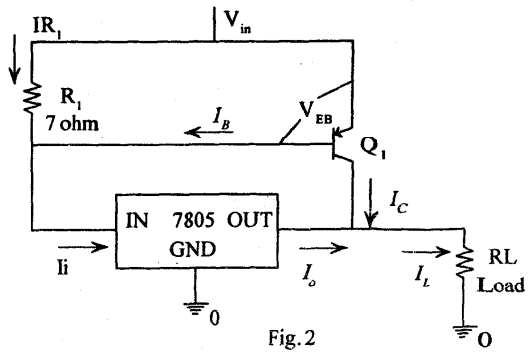

Fig. 2

4. (*a*) Draw the circuit diagram of logarithmic amplifier and explain its operation. 8

(*b*) Draw the output waveform for a square wave of 1V peak at 100 Hz applied to the differentiator. 2

(*c*) Design a wide band pass filter having $f_L = 400$ Hz, $f_H = 2$ kHz and pass band gain of 4. Find the value of Q for the filter? 6

(*d*) Briefly explain about the applications of comparator. 4

Group B

5. (*a*) Explain the operation of non-stable multivibrator using op amp, and derive the expression for ON and OFF state time periods. 12

(*b*) In a voltage controlled oscillator, applied control voltage is 3 V, timing resistor, $R_t = 5$ k Ω, timing capacitor $C_t = 10$ μF. Find the frequency of oscillation. 3

(*c*) Determine the value of R_f necessary for the circuit shown in Fig. 3 to operate as an oscillator and find the frequency of oscillation. 5

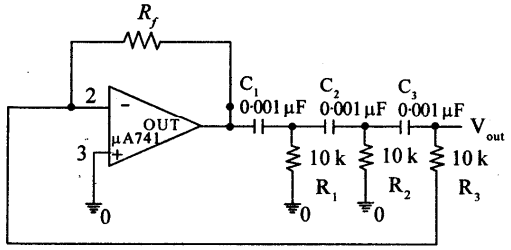

Fig. 3

6. (*a*) Explain how PLL can be used in frequency multiplier and AM detector circuits. 10

(*b*) With reference to a PLL, define capture range, lock range, and pull-in-time. 3 × 2

(*c*) Derive an expression for the output voltage in inverting summer. 4

7. (*a*) Calculate the values of LSB, MSB and full-scale output for an 8 bit DAC, if the applied input is in the range of 0 to 10 V range. 4

(*b*) Explain the operation of successive approximation analog-to-digital converter with a neat diagram. 12

(*c*) Define the parameter resolution and settling time of digital-to-analog converter. Obtain the value of resolution for an 8 bit DAC. 4

8. (*a*) In a digital voltmeter, a reference voltage of 2 V is used, if both $3\frac{1}{2}$ and $4\frac{1}{2}$ digit DVM are used. Calculate the resolution of DVM in both the cases and show which one gives better resolution ? 6

(*b*) Draw the circuit diagram of non-inverting integrator and explain in detail about its frequency response characteristics. 10

(*c*) Briefly explain the operation of sample-and-hold circuit. 4

Group C

9. Choose the *correct* answer for the following : 10 × 2

(*i*) A non-stable multivibrator has

(*a*) both the states as stable states.

(*b*) makes transition from one state to another when the trigger applied.

(*c*) both the states as unstable states.

(*d*) one stable state and one quasi-stable state.

(*ii*) IC LF 198 is an example of

(*a*) sample-and-hold circuit.

(*b*) log amplifier.

(*c*) antilog amplifier.

(*d*) voltage-to-frequency converter.

(*iii*) A non-inverting amplifier has input resistance $R_1 = 100\ \Omega$ and feedback resistance $R_f = 10\ k\Omega$. Its gain value is

(*a*) 10

(*b*) 101

(*c*) - 100

(*d*) - 200

(*iv*) The important feature of instrumentation amplifier is

(*a*) low CMRR.

(*b*) high output impedance.

(*c*) high gain stability.

(*d*) high d.c. offset.

(*v*) The output produced by ideal differentiator is

(*a*) $V_0 = -R_f C_1 \, dV_i/dt$

(*b*) $V_0 = (-1/R_f C_1)(dV_i/dt)$

(*c*) $V_0 = (-R_f C_1)(dI_i/dt)$

(*d*) $V_0 = (-1/R_f C_1)(dI_i/dt)$

(*vi*) The other name of one shot vibrator is

(*a*) Schmit trigger.

(*b*) monostable multivibrator.

(*c*) bistable multivibrator.

(*d*) astable multivibrator.

(*vii*) Which one of the following is true for narrow band pass filter ?

(*a*) $Q < 10$

(*b*) $Q > 10$

(*c*) $Q < 5$

(*d*) $Q = 1$

(*viii*) The time period of IC 555 monostable multivibrator operation is

(*a*) 1·38 RC

(*b*) 1·1 RC

(*c*) 1·45 RC

(*d*) 13·8 RC

(*ix*) The number of frequencies produced at the output of binary FSK modulator is

(*a*) two.

(*b*) infinite.

(*c*) power of two.

(*d*) three.

(*x*) The basic step of 4 bit DAC is 10 mV. If 0000 represents 0 V, what is the output produced, if the input is 1011 ?

(*a*) 110 mV

(*b*) 11 mV

(*c*) 110 mV

(*d*) 1·1 mV

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Group A

1. (*a*) Why is it that BIFET operational amplifiers have extremely low input bias current levels ? 3

(*b*) Describe two methods of offset nulling that might be used with a 741 op amp. 5

(*c*) Sketch the circuit of an op amp difference amplifier and derive an expression for the output in terms of the input. 6

(*d*) Design a capacitor-coupled voltage follower using a 741 op amp. The lower cut-off frequency of the circuit is 70 Hz and load = 4 kΩ. 6

2. (*a*) Distinguish between a dual and a dual tracking regulated power supply. 4

(*b*) Why is it desirable for a power supply to have a low output impedance ? 3

(*c*) What is the purpose of a bleeder resistance ? With reference to a bleeder resistance, why are carbon resistors preferable to wire wound resistors ? 5

(*d*) A half wave rectifier output is smoothed by a capacitor C and 20 V is fed to a load of 500 ohm. Maximum ripple amplitude is 10 per cent of the average output voltage. The input frequency is 60 Hz. Determine the value of C. 8

3. (*a*) Draw the circuit diagram of a simple Zener diode voltage regulator and explain how the circuit operates. 4

(*b*) Sketch a foldback current limiting circuit for a voltage regulator and explain the operation of the circuit. 5

(*c*) How can current boost be obtained in a three terminal regulator ? 14

(*d*) Using LM 217, design a IC voltage regulator to provide a 6 V fixed output. The supply voltage is 15 V. 7

4. (*a*) List the basic differences between Norton's amplifier and conventional op amp. 4

(*b*) Explain how a multiplier can be built using log amplifiers. 4

(*c*) Draw the circuit diagram of a dual op amp instrumentation amplifier. What is its drawback when it is compared with the triple op amp instrumentation amplifier ? 4

(*d*) Design a Sallen-Key unity gain low pass active filter to meet the following requirements : (*i*) Roll of rate = – 40 dB/decade, (*ii*) pass band as flat as possible, (*iii*) cut-off frequency = 2 kHz, and (*iv*) gain at DC = 5. 8

Group B

5. (*a*) Draw the circuit diagram of a Hartley oscillator and derive an expression for the frequency of oscillation. 5

(*b*) Describe procedures for stabilising the amplitude of the output of an oscillator. 6

(*c*) Why does the frequency stability of a clapp oscillator increase as g_m increases ? 3

(*d*) Design a Wein bridge oscillator whose frequency of oscillation f_0 is 625 Hz. 6

6. (*a*) Explain how a monostable multivibrator can be used to detect a missing pulse. 5

(*b*) Explain how a triangular wave can be converted into a sine wave. 5

(*c*) State the important features of grounded capacitor voltage-controlled oscillators and emitter-coupled voltage-controlled oscillators. 3

(*d*) Using a 555 timer, design an astable multivibrator. Given : frequency $f_0 = 50$ kHz and duty cycle $D = 75$ per cent. 7

7. (*a*) Show that, for tone modulated AM, the maximum efficiency is 33 per cent. 4

(*b*) Explain how a DSB-SC signal can be demodulated by carrier re-insertion and envelope detection. 6

(*c*) Using a neat block diagram, explain how a PLL can be used as a FSK demodulator. 5

(*d*) Select filter components for a PLL whose lowest frequency from the phase detector is 5 Hz. A 0·5 percent variation in frequency is allowable. 5

8. (*a*) Convert the base 3 number 1021121·121 directly into a base 9 number. Do not convert to base 10 number. 3

(*b*) Draw and explain the block diagram of a ramp-type digital voltmeter. 7

(*c*) Show that the NOR gate is a universal building block. 4

(*d*) Using a neat sketch, explain the working of a parallel comparator (flash) analog-to-digital converter. 6

Group C

9. Choose the *correct* answer for the following : 10 × 2

(*i*) In a cascaded differential amplifier,

(*a*) RC coupling is used.
(*b*) direct coupling is used.
(*c*) AC coupling is used.
(*d*) AC or DC coupling may be used.

(*ii*) How many op amps does a window comparator require ?

(*a*) 1
(*b*) 2
(*c*) 3
(*d*) 4

(*iii*) A multiplier, which can accept input voltage of any polarity and can produce output voltages of any polarity, is called

(*a*) universal multiplier.
(*b*) one quadrant multiplier.
(*c*) two quadrant multiplier.
(*d*) four quadrant multiplier.

(*iv*) Thermal shutdown in 78 XX will occur at

(*a*) 70 °C
(*b*) 90 °C
(*c*) 110 °C
(*d*) 135 °C

(*v*) The output voltage of a switching regulator for an input V_{in} and duty cycle δ is given by

(*a*) $V_{in}\,\delta$
(*b*) $V_{in}(1-\delta)$
(*c*) $V_{in}(1-\delta)/\delta$
(*d*) $V_{in}\,\delta/(1-\delta)$

(*vi*) Which one of the following is not a dual timer ?

(*a*) NE 556
(*b*) MC 3456
(*c*) MC 1422
(*d*) XR 2556

(*vii*) In order to use PLL in a frequency synthesizer, one additionally requires

(*a*) frequency counter.
(*b*) oscillator
(*c*) analog multiplier.
(*d*) high pass filter.

(*viii*) Second order filters, in which the damping factor exceeds 0·7, are called

(*a*) Butterworth filters.

(*b*) Chebyshev filters.
(*c*) Bessel filters.
(*d*) Sallen-Key filters.

(*ix*) Quantisation error in ADC or DAC is

(*a*) ± (1/2) LSB
(*b*) ± (1/2) V_{in}
(*c*) ± (1/2) V_{LSB}
(*d*) ± (1/2) V_0

(*x*) A positive logic AND gate is same as a

(*a*) negative logic AND gate.
(*b*) negative logic NAND gate.
(*c*) negative logic NOR gate.
(*d*) negative logic OR gate.

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Group A

1. (*a*) Explain, with help of circuit diagrams, the followings which are related to op-amp : (*i*) Virtual ground, (*ii*) CMRR, (*iii*) PSRR, (*iv*) input bias current. 4 × 2

   (*b*) Draw an inverting op-amp integrator circuit and its equivalent circuit. Find the expression for output voltage of the non-inverting integrator. 7

   (*c*) Describe universal offset voltage balancing technique for an op-amp. 5

2. (*a*) Explain the working principle of a regulated power supply using Zener diode over the range of input voltage variation V_{min} to V_{max}. 7

(*b*) Draw a full-wave rectifier with a capacitor filter and derive the expression for ripple power. **8**

(*c*) Explain the principle of UPS operation. 5

3. (*a*) Draw the circuit of a half-wave rectifier using IC 741 op-amp with positive input and find the expression for output voltage. 10

(*b*) Explain the working principle of a feedback limiter circuit. 4

(*c*) What is short circuit protected regulator and dual tracking regulator ? 6

4. (*a*) Difference mode gain of a DIFF AMP is $A_d = 2000$. Calculate the output voltages for (*i*) CMRR = 100, and (*ii*) CMRR = 10,000, if the inputs are $V_1 = +1{\cdot}0$ mV and $V_2 = +0{\cdot}9$ mV and show the effect of high CMRR. Assume V_i applied at 1 mV input. 5

(*b*) Find the expression for overall output voltage of a differential amplifier with three op-amps. 8

(*c*) Find the expression for output voltage of a logarithmic amplifier and design a two input multiplier. 4

(*d*) Draw the zero-crossing detector ? Explain its function. 3

Group B

5. (*a*) Draw the circuit diagram of a RC-phase shift oscillator using op-amp and obtain the frequency of oscillation. 12

(*b*) Describe the working principle of a function generator that gives square wave and triangular wave of same frequency. 4

(*c*) What is VCO ? How does it get represented, say f_c, in transfer function form ? 4

6. (*a*) What is a square law detector ? Explain with a block diagram. How does it work for a selected range of frequencies ? 7

(*b*) What is a DSB-SC system ? Explain how, using balanced modulator, DSB-SC signal can be generated. How does it differ in shape from 100 % AM ? 8

(*c*) What is synchronous detection ? How is synchronous detection affected by phase error and frequency error ? How can you obtain coherent carrier at receiver for this circuit ? 5

7. (*a*) Describe the principle of working of a R-2R digital-to-analog converter. What is the minimum and maximum values of gain for it ? How can a digital-to-analog converter be used as current-to-voltage converter ? 10

(*b*) Draw the block diagram of an astable multivibrator using op-amps and explain its working principle. 5

(*c*) What is a digital frequency synthesizer ? How can a desired frequency be obtained from it ? 5

8. Write notes on the following : 8 + 6 + 6

(*a*) Video amplifier

(*b*) Digital voltmeter

(*c*) Frequency multiplier.

Group C

9. Choose the *correct* answer for the following : 10 × 2

(*i*) Output of an inverting op-amp is 10 sin *wt*. Slew rate of the amplifier is

(*a*) W
(*b*) 10
(*c*) 10 W
(*d*) 10 cos wt.

(*ii*) The range of time, within which a degree of certainty can be determined between a true value and an estimated value of communicating signals, is known as

(*a*) confidence interval.
(*b*) delay interval.
(*c*) hopping time.
(*d*) spreading time.

(*iii*) GMSK is a special care of

(*a*) QAM
(*b*) FSK
(*c*) QPSK
(*d*) PSK

(*iv*) The circuit used to convert FM signal into its corresponding AM siganl, with the help of a frequency dependent circuit, is known as

(*a*) encoder.
(*b*) decoder.
(*c*) frequency discriminator.
(*d*) slope detector.

(*v*) If input resistance is infinite and feedback resistance is zero, then a non-inverting op-amp acts as a

(*a*) integrator.
(*b*) differential amplifier.
(*c*) inverting op-amp.
(*d*) voltage follower.

(*vi*) In a ROM memory of sixteen 8-bit words, 16 memory elements are arranged in a 4 × 4 array. This topology is called

(*a*) coincident selection.
(*b*) matrix selection.
(*c*) linear selection.
(*d*) parallel selection.

(*vii*) An AM transmitter has carrier power output of 50 W. Total power produced with 80% modulation is

(*a*) 66 W
(*b*) 60 W
(*c*) 40 W
(*d*) 86 W

(*viii*) For a filter, when the transition band between passband and stopband is very narrow, it is known as

(*a*) soft roll-off.
(*b*) hard roll-off.
(*c*) slow roll-off.
(*d*) fast roll-off.

(*ix*) The sampler, which uses sampling and hold circuit, is called

(*a*) flat top sampling.
(*b*) natural sampling.
(*c*) ideal sampling.
(*d*) switching sampling.

(*x*) If two different cascaded tuned amplifier circuits are tuned to slightly different frequencies to obtain increased bandwidth with a flat passband and steep sides, the technique is known as

(*a*) double-tuned.
(*b*) flat-tuned.
(*c*) stagger-tuned.
(*d*) frequency-tuned.

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Group A

1. (*a*) Using an op amp, explain how you will build a negative resistance converter. Derive an expression for the negative resistance that is simulated. **8**

(*b*) Using a T-network and an op amp, draw the circuit diagram of a high sensitivity I - V converter. Explain the need for JFET input and MOSFET input op amps in a high sensitivity I - V converter. **6**

(*c*) Describe offset nulling for a LM 311 voltage comparator using a neat sketch. **6**

2. (*a*) Draw the circuit diagram of a precision half wave rectifier and explain how it works. **6**

(*b*) A 10 V precision voltage reference has a maximum thermal coefficient of 1 ppm/°C. Find the variation in output voltage when the temperature changes from 0°C to 70°C. 4

(*c*) With reference to a regulator, describe short-circuit protection and current fold-back protection. 7

(*d*) How does a switching regulator achieve higher efficiency ? 3

3. (*a*) Draw the schematic diagram of an analog multiplier using logarithmic amplifier made of op amps. 10

(*b*) Design a two input amplifier with CMRR = 500 using op-amp with ideal characteristics. 10

4. (*a*) Explain how ground loop interference can be eliminated using a difference amplifier. 4

(*b*) State the relative merits of triple op amp instrumentation amplifiers and dual op amp instrumentation amplifiers. 4

(*c*) Design a low pass first order active filter to meet the following specifications : (*i*) - 3 dB frequency of 1 kHz, (*ii*) d.c. gain = 20 dB and (*iii*) input resistance ≥ 10 k Ω. 3 × 4

Group B

5. (*a*) Draw the circuit diagram of an op amp based Wien bridge oscillator and derive an expression for the frequency of oscillation. 7

(*b*) Explain how a limiter can be used to stabilise amplitude in a Wien bridge oscillator. 4

(*c*) Using 555 timer, design a free running multivibrator for a frequency f_0 = 50 kHz and duty cycle D = 75 percent. 6

(*d*) State the advantages of emitter-coupled voltage controlled oscillator. 3

6. (*a*) Draw and explain the circuit diagram of a CMOS crystal oscillator. Why does it have high degree of frequency stability ? 8

(*b*) Using neat sketches, describe (*i*) triangular to sine wave converter and (*ii*) sine wave to triangular wave converter. 6

(*c*) Design a ICL 8038 waveform generator for a frequency f_0 = 10 kHz. Assume V_{cc} = 15 V. 6

7. (*a*) What is the need for pre-emphasis ? Explain the working of pre-emphasis and de-emphasis circuits in public address system. 7

(*b*) A carrier signal of 600 V RMS is applied to a 75 ohm antenna. What is the carrier power ? Determine the total sideband power and total radiated power at 75 percent amplitude modulation. 5

(*c*) Using neat sketches, explain how the *p-n* junction can be used to design voltage to frequency converter ? 4

(*d*) State and prove Nyquist's sampling theorem. 4

8. (*a*) Using a neat sketch, describe the working of a weighted capacitor D/A converter. 8

(*b*) What are the two reasons on account of which $\Sigma - \Delta$ A/D converters use feedback ? 4

(*c*) Show that a positive logic AND gate is the same as a negative logic OR gate. 4

(*d*) Write the truth tables for half subtractor and full subtractor. 4

Group C

9. Choose the *correct* answer for the following : 10 × 2

(*i*) A 741 inverting amplifier with a gain of –2 is driven by a ± 10 V peak-to-peak triangular wave as shown in Fig. 1:

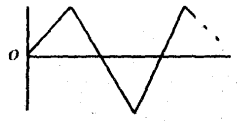
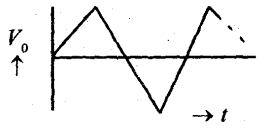


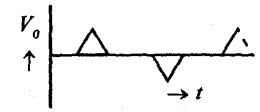
Fig. 1

The waveform at the output will be

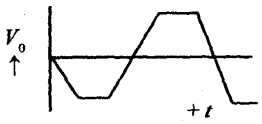
(*a*)



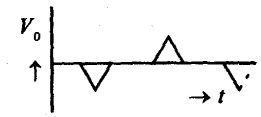
(*b*)



(*c*)



(*d*)



(*ii*) CMRR in dB is given by

(*a*) $10 \log_{10}(A_{dm}/A_{cm})$

(*b*) $10 \log_{2}(A_{dm}/A_{cm})$

(*c*) $10 \log_{e}(A_{dm}/A_{cm})$

(*d*) $20 \log_{10}(A_{dm}/A_{cm})$

(*iii*) KRC filters are also called

(*a*) passive filters,

(*b*) notch filters.

(*c*) all pass filters.

(*d*) Sallen key filters.

(*iv*) For a track and hold amplifier, the feed through rejection ratio = 80 dB. The hold mode voltage changes by 10 V. The change in output voltage equals

(*a*) 1 mV

(*b*) 2 mV

(*c*) 10 mV

(*d*) 20 mV

(*v*) For a quadrature oscillator, the frequency of oscillator is given by

(*a*) 2 ΠRC

(*b*) 1/(2 ΠRC)

(*c*) $1/(\sqrt{6}\ \Pi RC)$

(*d*) 1/(ΠRC)

(*vi*) The output voltage of a regulator changes by 3 mV when the input is varied from 7 V to 25 V. Its line regulation is equal to

(*a*) 0·17 mV/V

(*b*) 6 V/mV

(*c*) 54 mV/V

(*d*) 18·003 mV/V

(*vii*) Consider a DAC based A/D converter. To convert a full scale input, a 12 bit ADC with a 1 MHz counter clock will need

(*a*) 4·096 ns

(*b*) 4·096 μs

(*c*) 4·095 ms

(*d*) 40·95 ms

(*viii*) The maximum carrier frequency change for FM broadcast radio is given to be ± 75 kHz. An FM broadcast carrier is deviated by ± 30 kHz. The percentage of modulation is

(*a*) 25

(*b*) 40

(*c*) 30

(*d*) 75

(*ix*) The maximum VCO frequency of CMOS PLLs is typically of the order of

(*a*) 10 kHz

(*b*) 100 kHz

(*c*) 10 MHz

(*d*) 20 MHz

(*x*) The outputs of two 2-input NOR gates are cross-coupled. The result is a

(*a*) D flip-flop

(*b*) T flip-flop

(*c*) JK flip-flop

(*d*) SR flip-flop

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Group A

1. (*a*) Design a 3-op amp high input impedance instrumentation amplifier and derive an expression for its output voltage (V_0) in terms of the *i/p* voltages V_2 and V_1. Briefly explain its operation. 8 + 4

   (*b*) Design a single op-amp logarithmic amplifier and derive the relation between the *o/p* and *i/p* voltage to explain why it is called a logarithmic amplifier. How can we say that the amplifier design is for $V_0 = \log_{10} V_i$? 8

2. (*a*) In an op-amp, if the first set of inputs are + 50 μV and − 50 μV and the second set of inputs are 950 μV and 1050 μV and if the CMRR = 100, calculate the percentage difference in two output signals for two sets of inputs. Repeat the calculation, if CMRR = 10,000. 10

(*b*) Design a single op amp non-inverting integrator circuit, explain its operation and derive the input-output relation. Does the output resemble the output of inverting integrator with polarity inverted ? 8 + 2

3. (*a*) For the diagram shown in Fig. 1, calculate the break points and sketch the transfer characteristics. Assume ideal diodes : 15

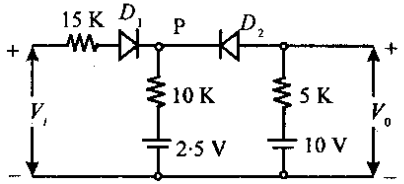


Fig. 1

(*b*) For a 2-diode full-wave rectifier circuit, sketch the o/p current and derive the expression for d.c. and rms values of the load current. What will be the value of d.c. current, if a voltage regulator is used ? 1 + 2 + 2

4. Write short notes on the following : 2 × 10

(*a*) Zero cross-over detector

(*b*) Polyphase rectifier.

Group B

5. (*a*) State the Barkhausen criterion for frequency of oscillation and condition of its sustenance. How can a voltage controlled oscillator be designed ? 3 + 3

(*b*) Give the generic form of an oscillator. Identify the amplifier (gain) block and the phase shifting network in it. Derive an expression for loop gain, AB, for this oscillator. 10

(*c*) What do you mean by Colpitt's oscillator ? How does it differ from that of Hartley oscillator ? 4

6. (*a*) Describe the operation of a 4-bit dual slope AD converter with a supporting block diagram. How many clock cycles will be needed for digital conversion of a sample in it ? 14

(*b*) Briefly present the structure of a DA converter using binary weighted resistors and state its disadvantages. Show that for 8-bit A/D converter of this type, 10 clock pulses are needed as triggers. 6

7. (*a*) For the circuit shown in Fig. 2, calculate the stable-state currents and voltages. Assume $h_{FE}|_{min} = 20$ and $V_{BE}|_{sat} = V_{CE}|_{sat} = 0$ for Si-transistor. 15

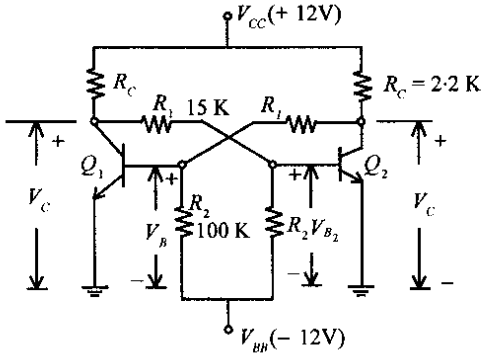


Fig. 2

(*b*) Design the aforesaid circuits by op-amp replacing the transistors. 5

8. (*a*) Explain the operation of a square law demodulator and derive the mathematical expression recovering the

original unmodulated signal. How can a diode in linear rectifier region of characteristic demodulate AM signal ? 12

(*b*) What is PSK ? What are its advantages over ASK and FSK ? Is it necessary to use phase locked loop for PSK demodulation ? 8

Group C

9. Answer the following in brief : 10×2

(*i*) A monostable multivibrator is also called a free-running multivibrator. (Yes/No)

(*ii*) A bistable multivibrator can act as a binary flip-flop. (Yes/No)

(*iii*) β of a transistor working in linear mode is the ratio of emitter current and collector current. (True/False)

(*iv*) Give the full form of FSK.

(*v*) FM transmission is less susceptible to environmental noise and interference. (True/False)

(*vi*) Estimate the delay in a 555 timer, if $R = 100$ kΩ and $C = 10$ μF.

(*vii*) Expand SSBSC.

(*viii*) In a voltage follower, if 100 mv sinusoid is given at the i/p, what shall be the o/p voltage ?

(*ix*) Expand PLL.

(*x*) Expand ALU.

S'15 : 7AN : EC 407 (1482)

DESIGN OF ELECTRONIC DEVICES AND CIRCUITS

Time : Three hours

Maximum Marks : 100

Answer FIVE *questions, taking* ANY TWO *from* **Group A,** ANY TWO *from* **Group B** *and* ALL *from* **Group C.**

All parts of a question (a,b,etc.) should be answered at one place.

Answer should be brief and to-the-point and be supplemented with neat sketches. Unnecessary long answers may result in loss of marks.

Any missing or wrong data may be assumed suitably giving proper justification.

Figures on the right-hand side margin indicate full marks.

Group A

1. (*a*) Draw a neat sketch showing the P-spice model of an ideal op amp. **4**

(*b*) Derive the equivalent circuit of an op-amp by using Miller's theorem. **8**

(*c*) The non-inverting input and the inverting input of an op-amp are connected to 150 μV and 140 μV, respectively. The amplifier has a differential gain of 4000 and CMRR = 100. Determine the output voltage of the op-amp. **8**

2. (*a*) What does an unregulated power supply consist of ? State three disadvantages of an unregulated power supply. **4**

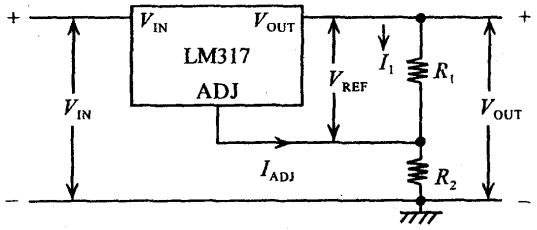
(*b*) Draw the circuit diagram of a semiconductor regulated power supply and explain its working. 10

(*c*) The stability factor, s_v, and the output resistance, R_0, of a regulated power supply are 0·022 and 0·51 Ω, respectively. Compute the change ΔV_0 in output voltage due to input voltage changes of ± 5 V and for a load currect I_L variation from 0 to 1 A. Assume that the temperature is constant. 6

3. (*a*) Distinguish between positive and negative voltage regulators. 4

(*b*) Draw a neat sketch showing a short-circuit overload protection circuit and explain its working. 8

(*c*) Consider the following LM317 adjustable voltage regulator :



Given : V_{REF} = 1·25 V and I_{ADJ} = 100 μA. Determine the regulated voltage when R_1 = 240 Ω and R_2 = 2·4 kΩ. 8

4. (*a*) Using three op-amps, draw the circuit diagram of an instrumentation amplifier and derive an expression for the output voltage. 8

(*b*) With the help of a circuit diagram, explain how an op-amp can be used to shift the phase of a sinusoidal input voltage while at the same time preserving its amplitude. 4

(*c*) Design a first order low pass active filter with a cut-off frequency of 6·63 kHz. Use a capacitance of 0·02 μF. The voltage gain below the cut-off frequency is constant at 5. 8

Group B

5. (*a*) Draw the circuit diagram of a FET phase shift oscillator. Show that a FET with a $\mu < 29$ cannot be made to oscillate in such a circuit. 7

(*b*) State piezoelectric effect. Draw the electrical equivalent circuit of a crystal and explain why a crystal can have two resonant frequencies. Sketch a graph showing crystal impedance against frequency. 1 + 1 + 2 + 2

(*c*) Design a Wien bridge oscillator for operation at f_0 = 10 kHz. 7

6. (*a*) Show that, in a balanced AM modulator, the carrier is suppressed. 7

(*b*) State the relative merits of AM, DSB-SC and SSB-SC systems. 4

(*c*) Why is coherent or synchronous demodulation of AM rarely used in practice ? 3

(*d*) Determine the percentage of the total power carried by the sidebauds of an AM wave for tone modulation when the modulation index μ = 0·5. 6

7. (*a*) Draw and explain the block diagram of a super-rheterodyne receiver. 6

(*b*) Why is the intermediate frequency (IF) selected as 455 kHz ? 4

(*c*) With reference to FM, what is 'capture effect' ? 3

(*d*) The PLL 565 is connected to work as an FM demodulator. Resistor R_1 and capacitor c_1, which determine the free running frequency f_0, are 10 kΩ and 220 pF, respectively. Supply voltage is ± 6 V. Determine the free running frequency f_0 and the lock range f_L. 7

8. (*a*) Show that the NOR gate is a universal building block. 3

(*b*) Draw the block diagram of a ramp-type digital voltmeter and explain its working. 8

(*c*) Explain why dual slope ADC provides noise rejection. 4

(*d*) What is the output voltage provided by a 4 bit DAC when the input binary number is 0110. The output voltage range of the DAC is 0 to 10 V. 5

Group C

9. Choose the *correct* answer for the following : 10 × 2

(*i*) An example of a military grade op-amp with higher slew rate is

(*a*) 741
(*b*) 741 A
(*c*) 741 C
(*d*) 741 S

(*ii*) A non-inverting amplifier, with a gain of 100, is nulled at 25 °C. What will be the change in the output voltage, if the temperature rises to 45 °C for an offset voltage drift of 0·15 mV/°C ?

(*a*) 375 mV
(*b*) 300 mV
(*c*) 3·75 mV
(*d*) 3 mV

(*iii*) The input to an op-amp is a square wave. The output of the op-amp voltage follower rises from − 3 V to + 3V in 0·25 μs. The slew rate of the op-amp is

(*a*) 1·2 V/μs
(*b*) 2·4 V/μs
(*c*) 14 V/μs
(*d*) 24 V/μs

(*iv*) Consider a lossy integrator. The component values are R_1 = 10 kΩ, R_F = 100 kΩ and S_F = 10 nF. The lower frequency limit of integration is

(*a*) 10 Hz
(*b*) 16 Hz
(*c*) 159 Hz
(*d*) 1·59 kHz

(*v*) An example of a positive voltage regulator is

(*a*) LM 217
(*b*) LM 137
(*c*) LM 237
(*d*) LM 337

(*vi*) Determine the order of a low pass Butterworth filter that provides 40 dB attenuation at $w/w_n = 2$ is

(*a*) 5
(*b*) 6
(*c*) 7
(*d*) 8

(*vii*) A positive logic AND gate is the same as a negative logic

(*a*) AND gate
(*b*) OR gate
(*c*) NAND gate
(*d*) NOR gate

(*viii*) In order to build a MOD-30 counter, the minimum number of flip-flops needed is

(*a*) 30
(*b*) 15
(*c*) 10
(*d*) 5

(*ix*) A Schmitt trigger converts slowly varying wave-forms into

(*a*) square wave.
(*b*) sine wave.
(*c*) sawtooth wave.
(*d*) triangular wave.

(*x*) The broadcast baud AM radio uses the baud

(*a*) 55 MHz TO 160 MHz
(*b*) 5·5 MHz TO 16 MHz
(*c*) 550 kHz TO 1600 kHz
(*d*) 55 kHz TO 160 kHz

W'15: 7 AN : EC 407 (1482)

DESIGN OF ELECTRONIC DEVICES AND CIRCUITS

Time : Three hours

Maximum Marks : 100

Answer FIVE *questions, taking* ANY TWO *from* **Group A,** ANY TWO *from* **Group B** *and* ALL *from* **Group C.**

All parts of a question (a,b,etc.) should be answered at one place.

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Group A

1. (*a*) Why is R_E replaced by a constant current bias circuit in a differential amplifier ? 5

   (*b*) Why is the cascade configuration used in an op amp ? 5

   (*c*) State the advantages of MOSFET op amps over BJT op amps. 4

   (*d*) For 741 C, the maximum internal capacitor charging current is limited to 15 μA. The compensating capacitor is 30 pF. Determine the slew rate of the op amp 741 C. 6

2. (*a*) State the relative merits of linear power supply and switched mode power supply. 4

(*b*) For a power supply, sketch the short circuit, overload protection circuit and explain its operation. 8

(*c*) State three disadvantages of an unregulated supply. 3

(*d*) Calculate the value of inductance to be used in an inductor filter for a full wave rectifier operating at 60 Hz to provide a d.c. output with 4 percent ripple for a 100 Ω load. 5

3. (*a*) For a voltage regulator, define line regulation and load regulation. 4

(*b*) How does a Zener diode maintain constant output voltage ? 4

(*c*) State the limitations of three terminal regulators. 4

(*d*) Design a voltage regulator to give 6 V output for input fluctuations 10 V to 15 V. 8

4. (*a*) Distinguish between d.c. and a.c. amplifiers. 3

(*b*) Draw the circuit diagram of a voltage to current converter, if the load is (*i*) floating and (*ii*) grounded. Is there any limitation on the size of the load when the load is grounded ? 4

(*c*) Using a neat sketch, explain the working of a sample and hold circuit. What are the applications of sample and hold circuits ? 5

(*d*) Design a wideband pass active filter having the band pass from f_l = 400 Hz to f_h = 2 kHz and pass band gain of 4. 8

Group B

5. (*a*) Why do we need three RC networks in a phase shift oscillator ? Can it be two or four ? 4

(*b*) Distinguish between a sawtooth wave and a triangular wave. 4

(*c*) State the relative merits of RC and LC oscillators. 4

(*d*) In a Colpitts oscillator, c_1 = 0·2 μF and c_2 = 0·02 μF. If the frequency of oscillation is 10 kHz, find the value of the inductance. Find the required gain for oscillation. 8

6. (*a*) Explain the need for emitter resistor R_E in an emitter-coupled astable multivibrator. 4

(*b*) With reference to a Schmitt trigger, what is hysteresis voltage ? 4

(*c*) What are steering diodes ? Why are they needed ? 4

(*d*) Design a monostable multivibrator for a time delay T of 110 ms. 8

7. (*a*) Draw the circuit diagram of a typical two stage video amplifier and explain how it works. 8

(*b*) Explain how an AM signal can be demodulated using a square law detector. 4

(*c*) Draw the block diagram of a superheterodyne AM receiver. 4

(*d*) What is a PLL ? How does it work ? 4

8. (*a*) Draw the circuit diagram of a simple weighted resistor 3 bit D/A converter and sketch its transfer characteristics. 6

(*b*) How many comparators are needed in a 4 bit flash A/D converter ? 3

(*c*) How will you use an EX-OR gate as an inverter ? 3

(*d*) Draw the block diagram of a frequency meter (frequency counter) and explain its working. 8

Group C

9. Choose the *correct* answer for the following : 10 × 2

(*i*) The μA 747 is a dual 741 and is available in

(*a*) 10 pin can only.

(*b*) 14 pin DIP only.

(*c*) 10 pin can or 14 pin DIP.

(*d*) flat pack.

(*ii*) The N5741 op amp is manufactured by

(*a*) national semiconductor.

(*b*) RCA.

(*c*) Texas instruments.

(*d*) Signetics.

(*iii*) A voltage follower may be used to connect

(*a*) low impedance source to a low impedance load.

(*b*) high impedance source to a low impedance load.

(*c*) low impedance source to a high impedance load.

(*d*) high impedance source to a high impedance load.

(*iv*) A full wave rectifier delivers 50 W to a load of 200 Ω. If the ripple factor is one percent, the a.c ripple voltage across the load is

(*a*) 1 V

(*b*) 2 V

(*c*) 3 V

(*d*) 4 V

(*v*) I to V converters are used in

(*a*) testing of photo devices.

(*b*) low voltage d.c. voltmeters.

(*c*) low voltage a.c. voltmeters.

(*d*) Zener diode testers.

(*vi*) An example of a negative resistance oscillator is

(*a*) Clapp oscillator.

(*b*) tunnel diode oscillator.

(*c*) Franklin oscillator.

(*d*) Armstrong oscillator.

(*vii*) The hexadecimal equivalent of the decimal number 1195 is

(*a*) 4 ABC

(*b*) 4 AC

(*c*) 4 BC

(*d*) 4 AB

(*viii*) The Gray code corresponding to the binary number 0101 is

(*a*) 0101

(*b*) 1010

(*c*) 1111

(*d*) 0111

(*ix*) Consider a 3-1/2 digit DVM. The reference voltage is 2 V. Its resolution is

(*a*) 3 mv

(*b*) 2 mv

(*c*) 1 mv

(*d*) 0·5 mv

(*x*) All digital voltmeters use

(*a*) successive approximation ADC.

(*b*) dual slope ADC.

(*c*) parallel comparator ADC.

(*d*) tracking ADC.

S'16 : 7 AN : EC 407 (1482)

DESIGN OF ELECTRONIC DEVICES AND CIRCUITS

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Group A

1. (*a*) What is an integrated circuit ? How does it differ from a discrete circuit ? Discuss the relative merits and demerits of ICs over discrete circuits. 7

   (*b*) Draw the circuit diagram of a full-wave rectifier using two diodes and calculate (*i*) I_{dc}, (*ii*) I_{ms} and (*iii*) PIV rating of diode. 7

   (*c*) The slew rate of an op-amp is 6 V/μs when closed-loop gain is unity. The amplified output signal is observed to be a pure sinusoid, $v_{out} = V_{max} \cos \omega t$ provided the frequency of this signal does not exceed a certain limit. Find the value of this limiting frequency before the output signal is distorted by the slew rate limit, if (*i*) $V_{max} = 1$ V and (*ii*) $V_{max} = 10$ V. 3 + 3

(Turn Over)

2. (*a*) Discuss the limitations of linear voltage regulators. Explain switch-mode power supplies. Discuss its advantages. 7

(*b*) What is UPS ? Why is the UPS system becoming more and more popular nowadays ? Compare online UPS, off-line UPS and electronic generator. 7

(*c*) Explain 'foldback current limiting' technique. How does it eliminate the limitation of constant current limiting circuit. 6

3. (*a*) Derive the expression for differential mode gain of a differential amplifier. Describe the advantages of a differential amplifier as regards to noise immunity and drift immunity. 7

(*b*) Design a voltage regulator to give 6 V output for input fluctuations from 10 V to 15 V for Zener breakdown current 5 mA < I < 15 mA. 7

(*c*) Explain the working of a basic logarithmic amplifier using op-amps. Design a voltage multiplier with this technology. 6

4. (*a*) Where are sample and hold circuits used ? Sketch the circuit arrangement along with output waveform and discuss briefly the operation of the circuit. How can the hold time be controlled ? 7

(*b*) Why is an instrumentation amplifier called so ? Describe the operation of an instrumentation amplifier. 5

(*c*) A 10 mV, 2 kHz sinusoidal signal is applied to the inverting input terminal of an op-amp integrator for which R = 50 kΩ and C = 2 μF. Determine the output voltage. What will happen, if connections at inverting terminal and non-inverting terminal are interchanged in the above circuit ? 8

Group B

5. (*a*) What is a phase shift oscillator ? How does it differ from an amplifier ? Derive an expression for frequency of oscillation. 7

(*b*) What is a monostable multivibrator ? Explain the stable state of this multivibrator. How spikes in output get averaged out ? 7

(*c*) Draw the diagram of triangular-wave generator using op-amp and find an expression for the frequency of oscillation. Can the triangular wave have dual slope and single slope as per the design ? Explain how ? 6

6. (*a*) What is a cascade amplifier ? Determine the performance of a cascade amplifier. Hence, find y-parameter for the same. What is its advantage over that of cascade amplifier ? 7

(*b*) Draw a simplified schematic of balanced modulator and demodulator. Find the limitation of envelope detection in this case. 7

(*c*) Explain, with a neat diagram, the working of a frequency multiplier. 6

7. (*a*) Draw the circuit diagram of a typical digital voltmeter. How can it be modified for multiple range of measurements ? 7

(*b*) What is the basic principle of phase locked loop (PLL) ? Discuss the application of PLL. 7

(*c*) Draw a neat diagram for 4-bit R-2R ladder and weighted resistor-type D/A converters and compare them. How can D/A stage help in A/D converter design in some cases ? 6

8. (*a*) Explain the working of a three-digit dual-slope A/D converter. 7

(*b*) Draw the block diagram of a frequency meter (frequency counter) and explain its working. 5

(*c*) Determine the output voltage caused by each bit in a 6-bit ladder, if the input levels are 0 = 0 V and 1 = + 16 V. Determine the resolution and full-scale output of this circuit. Calculate the voltage from the above ladder for a digital input of 101011. 8

Group C

9. Choose the *correct* answer for the following : 10 × 2

(*i*) Consider the following statements :

(I) A differential amplifier is used at the input stage of an operational amplifier.

(II) Differential amplifiers have very high CMRR.

Of these two statements,

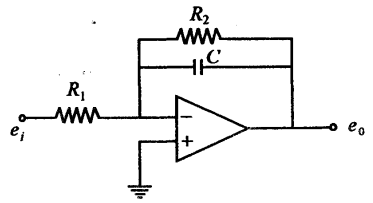
(*a*) both of these two statements, I and II, are true and statement II is the correct explanation of I.

(*b*) both I and II are true but statement II, is not the only explanation of I.

(*c*) I is true but II is false.

(*d*) I is false but II is true.

(*ii*) The op-amp shown below will be



(*a*) differentiator.

(*b*) integrator.

(*c*) non-inverting amplifier.

(*d*) integrator and inverting amplifier based on R_2 and C values.

(*iii*) A diac is a semi-conductor device which acts as a

(*a*) two terminal unidirectional switch.

(*b*) two terminal bidirectional switch.

(*c*) three terminal bidirectional switch.

(*d*) four terminal multidirectional switch.

(*iv*) A bridge rectifier provided with a shunt capacitor is connected to a 10 kΩ load. If the ripple factor is to be restricted to 0·01, the value of capacitor should be nearly

(*a*) 5 μF

(*b*) 10 μF

(*c*) 15 μF

(*d*) 30 μF

(*v*) In a.c. circuits, the a.c. meter measures

(*a*) r.m.s values.

(*b*) peak values.

(*c*) mean value.

(*d*) mean square values.

(*vi*) Blocking oscillators are used as

(*a*) abrupt pulse generators.

(*b*) low impedance switches.

(*c*) high impedance switches and frequency dividers.

(*d*) None of the three above.

(*vii*) A stable multivibrator produces

(*a*) pure sine waves.
(*b*) distorted sine waves.
(*c*) square waves.
(*d*) sawtooth voltages.

(*viii*) A class B amplifier is biased

(*a*) at cut-off.
(*b*) at nearly twice the cut-off bias.
(*c*) at mid-point of load line.
(*d*) such that I_B just equals I_C.

(*ix*) Which one of the following op-amp systems is a linear system ?

(*a*) Integrator
(*b*) Clipper
(*c*) Sample-and-hold circuit
(*d*) Logarithmic amplifier.

(*x*) Which one of the following hexadecimal numbers represents an odd decimal number ?

(*a*) FF
(*b*) EA
(*c*) CC
(*d*) AA

W'16: 7 AN : EC 407 (1482)

DESIGN OF ELECTRONIC DEVICES AND CIRCUITS

Time : Three hours

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Group A

1. (*a*) Explain how isolation between components is obtained in an IC. Also explain how are the components interconnected in an IC ? 4 + 2

(*b*) What is ion implantation ? Describe with a schematic diagram an ion-implantation system. What are the problems involved in an ion-implantation and how it can be overcome ? 1 + 4 + 2 + 1

(*c*) Using an op-amp, explain how you will build a negative resistance converter. Derive an expression for the negative resistance that is simulated. 6

2. (*a*) Draw the functional block diagram of an op-amp and

(Turn Over)

explain the operation of each block. Also write down the characteristics of an ideal op-amp. 4 + 2

(*b*) Define the terms (*i*) line regulation and (*ii*) load regulation related to a power supply. With a neat circuit explain how a regulated power supply can be designed using an op-amp and explain its operation. 2 + 6

(*c*) With reference to a regulator, describe short circuit protection and current fold back protection. 3 + 3

3. (*a*) Design a second order low pass Butterworth filter with a cut-off frequency of 1 KHz and a pass band gain of 4. Use a capacitor of value 0·01 μF. Also plot its gain frequency response. 8 + 2

(*b*) With a neat schematic explain the operation of a switching mode power supply(SMPS). Mention its advantage over a simple regulated dc supply. 8 + 2

4. Write notes on any *two* of the following : 2 × 10

(*a*) Instrumentation Amplifiers

(*b*) Logarithmic Amplifiers.

(*c*) Polyphase rectifier

(*d*) Programmable supply.

Group B

5. (*a*) Write down the condition for oscillation in an oscillator circuit. How oscillation builds up in any oscillator circuit ? 2 + 2

(*b*) With a neat schematic explain the operation of an R-C phase shift oscillator. Also derive expressions for its frequency of operation and condition for sustaining oscillation. 4 + 8

(*c*) Write down some advantage and disadvantages of a crystal oscillator. 4

6. (*a*) Design an astable multivibrator which has a frequency of oscillation of 10 kHz and duty cycle of 75%. Derive the necessary mathematical steps for the design. 8

(*b*) With a neat schematic explain the operation of a voltage controlled oscillator. Find out an expression for its frequency to show its dependency on input control voltage. Also derive an expression for its voltage to frequency conversion factor. 5 + 5 + 2

7. (*a*) Discuss with a neat circuit, the working of a Foster Seeley discriminator. 6

(*b*) The per cent modulation of an AM wave changes from 40% to 60%. Originally the power content at the carrier frequency was 900 W. Determine the power content at the carrier frequency and within each of the sidebands after the present modulation has risen to 60%. 6

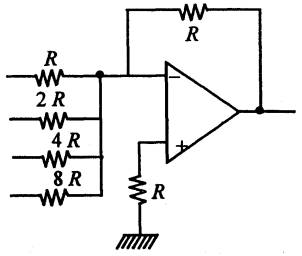
(*c*) Explain M-ary FSK system with the help of transmitters and receivers. Determine the bandwidth required for M-ary FSK system. 8

8. (*a*) With a neat schematic explain the operation of a dual slope type A/D converter. With necessary mathematical derivation prove that the value of the counter output is equal to the input analog voltage. 4 + 4

(*b*) Design a digital voltmeter using dual slope type A/D converter. 6

(*c*) Circuit of a 4 bit D/A converter is shown below. The input bits 0 and 1 are represented by 0 and 5 V respectively. The op-amp is ideal. All the resistors and

5V inputs have a tolerance of ± 10%. The specification (rounded to the nearest multiple of 5%) for the circuit. Calculate the tolerance of the *D* to *A* converter. 6



Group C

9. Choose the *correct* answer for the following : 10 x 2

(*i*) One of the following is not the characteristics of an ideal op-amp

(*a*) infinite voltage gain
(*b*) zero slew rate
(*c*) zero offset voltage
(*d*) infinite input impedance.

(*ii*) For a filter, when the transition band between pass-band and stopband is very narrow is known as

(*a*) soft roll-off
(*b*) hard roll-off
(*c*) show roll-off
(*d*) fast roll-off

(*iii*) In a series regulated power supply circuit, the voltage gain A_V of the 'pass' transistor satisfies the condition

(*a*) $A_V \rightarrow \infty$
(*b*) $1 \leq A_V < \infty$

(*c*) $A_V = 1$,
(*d*) $A_V << 1$

(*iv*) Speed up or commutating capacitor used in a bistable multivibrator to

(*a*) make the multivibrator state more stable.
(*b*) improve the resolution time.
(*c*) obtain time delay.
(*d*) Obtain a constant output swing.

(*v*) The schmitt trigger may be used to

(*a*) change voltage to corresponding frequency.
(*b*) change frequency to voltage.
(*c*) square a showly varying input.
(*d*) None of the three above.

(*vi*) The maximum number of comparators required to built an 8-bit flash ADC is

(*a*) 8
(*b*) 63
(*c*) 255
(*d*) 256

(*vii*) If the differential voltage gain and common mode voltage gain of a differential amplifier are 48 dB and 2 dB respectively, then its common mode rejection ratio is :

(*a*) 23 dB
(*b*) 25 dB
(*c*) 46 dB
(*d*) 50 dB

(*viii*) In a full wave rectifier using two diodes, V_{dc} and V_m are the dc and peak values of the voltage respectively across a resistive load. If PIV is the peak inverse voltage then appropriate relationship for this rectifier.

(*a*) $V_{dc} = V_m/\pi$; $PIV = 2V_m$

(*b*) $V_{dc} = 2V_m/\pi$; PIV = $2V_m$

(*c*) $V_{dc} = 2V_m/\pi$; PIV = V_m

(*d*) $V_{dc} = V_m/\pi$; PIV = V_m

(*ix*) The FM signal

$$10 \cos[2\pi \times 10^5 t + 5 \sin(2\pi \times 1500\, t) + 7{\cdot}5 \sin(2\pi \times 1000\, t)]$$

having carrier freq. of 10^5 Hz. The modulation index is

(*a*) 12·5

(*b*) 10

(*c*) 7·5

(*d*) 5

(*x*) Which of the following analog modulation scheme requires the minimum transmitted power and minimum channel bandwidth ?

(*a*) VSB

(*b*) DSB-SC

(*c*) SSB

(*d*) AM