ELECTRONIC CIRCUITS

***Time**: Three Hours*

***Maximum Marks**: 100*

Answer five questions, taking ANY TWO from Group A, any two from Group B and all from Group C.

All parts of a question (a, b, etc.) should be answered at one place.

Answer should be brief and to-the-point and be supplemented with neat sketches.

Unnecessary long answer may result in loss of marks.

Any missing or wrong data may be assumed suitably giving proper justification.

Figures on the right-hand side margin indicate full marks.

Group A

1. (a) Discuss the need for biasing a transistor. What do you mean by operating point? 6

   (b) Neatly draw the fixed bias circuit for an NPN transistor in CE configuration and explain its operation. Derive the expressions for its stability factors. 8

   (c) An NPN transistor is biased by collector-to-base bias method in CE mode. Given V_{BE} = 0.7 V, V_{CC} = 12 V, R_L = 2 kΩ, R_B = 100 kΩ and β = 99, find the quiescent point and three stability factors for reverse saturation current, temperature and p variations, respectively. 6

2. (a) Define the hybrid equivalent parameters for BJT in a common emitter configuration. Find the expression for current gain and input resistance of the CE amplifier in terms of the hybrid parameters. Are the h-parameters for a transistor constant? What do they vary with? 8

   (b) Derive the current gain (A_I), amplification of voltage (A_v), input impedance (Z_i) and output admittance (Y_0) in terms of h parameters and load resistance Z_L. If the source resistance R_s is taken into account how will the voltage amplification factor change. 8

   (c) Show that the voltage gain of a CS amplifier is given by $A_V = -\mu R_D/(r_d + R_D)$ 4

3. (a) Draw the circuit diagram of voltage series feedback amplifier and derive the expression for input and output impedance. 5

   (b) A negative feedback amplifier in voltage series configuration feeds 10% of the output back to the input. Voltage of the amplifier without feedback is 100. Input and output resistances are 10kΩ and 1kΩ respectively. Find percentage reduction in voltage gain, input resistance and output resistance with feedback. 5

   (c) Draw the functional block diagram of an op amp and mention the function of each block. 5

   (d) Draw the gain frequency response of an op-amp operating in open loop mode and explain how it can be changed using feedback. 5

4. (a) Design a circuit using op-amp that can give an average of four voltages 1V, 2V, 4V and 5 V at its input as its output. 6

   (b) What is the difference between a voltage amplifier and power amplifier? Draw the circuit diagram of a class A transformer coupled power amplifier and explain its operation. Derive all expression for its maximum efficiency. 8

   (c) With a neat sketch explain operation of class B push-pull amplifier. Show that the maximum conversion efficiency of an idealised class B push-pull circuit is 78.5%. 6

Group B

5. (a) Express the decimal number 416 in (i) excess three code (ii) BCD code (iii) binary code 5

   (b) Convert the following numbers: 5

   (i) $(0.513)_{10}$ to octal (ii) $(0.6875)_{10}$ to binary

   (c) What do you understand by “minterm” and “maxterm”? Discuss. 5

   (d) State and prove de Morgan’s theorem. Why is de Morgan’s theorem important in the simplification of Boolean expressions? 5

6. (a) Draw the circuit of 3 bit ripple (asynchronous) counter and explain its operation using timing diagram. 6

   (b) What is meant by modulus of a counter? Differentiate between 8

asynchronous and synchronous counter. Draw the logic diagram of a 4-bit ripple counter. Explain its working. Draw the corresponding state and timing diagram.

(c) Design a synchronous divide by 12 counter using JK flip flop. 6

7. (a) Write short note on shift counter. 4

(b) Design the circuit of a mod-7 asynchronous up counter using T-type flip flop. Write its truth table and draw its timing diagram for trailing edge trigger case. 8

(c) Explain how a decade counter can be built using four flip flops. 8

8. (a) Find the minimal SOP expression for the function 5

$$f(A,B,C,D) = \sum m(1,2,3,5,13) + \sum d(6,7,8,9,11,15)$$

Implement the minimised function using NAND gates.

(b) Minimize the following switching function on a Karnaugh map: 5

$$Y = \sum m(3,7,11,12,13,14,15) + \sum d(0,4)$$

(c) Give the truth table of (i) full adder (ii) half Subtractor. Give the logic realization using 2-input AND, OR, an INVERTER gates. 5

(d) Write truth table of full adder and obtain the expression for Sum and Carry. 5

Group C

9. Answer the following in brief: 20

(i) The main function of transformer used in the output of a power amplifier is

(a) To step up the voltage

(b) To increase the voltage gain

(c) To match the load impedance with dynamic output resistance of the transistor

(d) To safeguard the transistor against over heating

(ii) An op-amp is

(a) a differential amplifier

(b) a high gain push-pull amplifier

(c) a direct coupled amplifier

(d) a low impedance amplifier

(iii) A combinational circuit

(a) always contains memory elements

(b) never contains memory elements

(c) may sometimes contain memory elements

(d) contains only memory elements

(iv) A ring counter consisting of five flip-flops will have

(a) 5 states

(b) 10 states

(c) 32 states

(d) infinite states

(v) The BJT amplifier which offers highest input impedance and least voltage gain is

(a) CE

(b) CB

(c) CC

(d) cascade amplifier

(vi) Cascading of amplifiers results in

(a) increased gain and increased bandwidth

(b) increased gain and reduction in bandwidth

(c) increased input impedance decreased output impedance

(d) decreased input impedance and increased gain

(vii) Minimum number of two input NAND gates required to realize the logic function $(A\bar{B} + \bar{A}B)$ is

(a) 5

(b) 3

(c) 6

(d) 4

(viii) The multivibrator circuit which possesses one stable state and one quasi-stable state is

(a) astable

(b) monostable

(c) bi-stable

(d) Schmitt trigger circuit

(ix) Which of the following statement is not correct regarding h parameters of a transistor?

(a)Values of it parameters can be obtained from transistor characteristics

(b) Values depend on transistor configuration

(c) Values depend on operating point

(d) They are four in number

(x) Crystal oscillators are superior to tuned LC oscillators mainly because of their

(a) high degree of frequency stability

(b) size of the crystal

(c) availability of crystal

(d) high Q value

(Refer our course material for answers)